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1. **Force-directed scheduling for the behavioral synthesis of ASICs**
 Paulin, P.G.; Knight, J.P.;
[Computer-Aided Design of Integrated Circuits and Systems. IEEE Transactions on](#)
 Volume 8, Issue 6, June 1989 Page(s):661 - 679
 Digital Object Identifier 10.1109/43.31522
[AbstractPlus](#) | Full Text: [PDF](#)(1684 KB) IEEE JNL
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2. **Exploitation of instruction-level parallelism for optimal loop scheduling**
 Muller, J.; Fimmel, D.; Merker, R.;
[Interaction between Compilers and Computer Architectures. 2004. INTERACT-8 2004. Eighth Workshop on](#)
 15 Feb. 2004 Page(s):13 - 21
 Digital Object Identifier 10.1109/INTERA.2004.1299506
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